



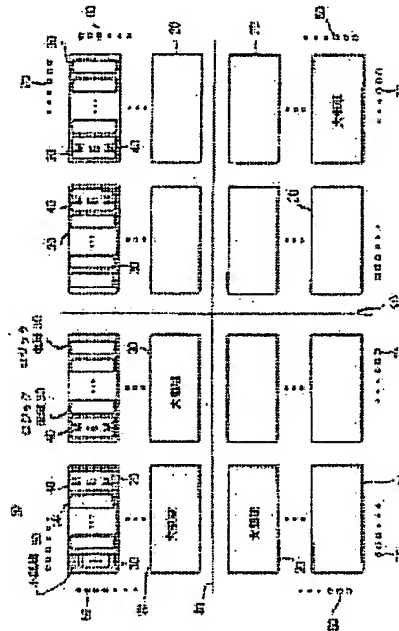


PROGRAMMABLE LOGIC DEVICE STRUCTURE**Publication number:** JP2000201066 (A)**Publication date:** 2000-07-18**Inventor(s):** JEFFERSON DAVID E; CAMERON MCCLINTOCK;
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RICHARD G; SURINIBASU T RED1**Applicant(s):** ALTERA CORP**Classification:****- international:** H01L21/82; H03K19/173; H03K19/177; H01L21/70;
H03K19/173; H03K19/177; (IPC1-7): H03K19/173;
H01L21/82**- European:** H03K19/177**Application number:** JP19990327549 19991117**Priority number(s):** US19980109417P 19981118; US19990266235 19990310**Also published as:**
 EP1005163 (A2)
 US2001006348 (A1)
 US6215326 (B1)
 DE69933525 (T2)
Abstract of JP 2000201066 (A)

PROBLEM TO BE SOLVED: To provide a large capacity programmable logic device structure capable of eliminating the need for any excessive amount of interconnection conductor resources on a device. **SOLUTION:** In a programmable logic device 10, plural large areas 20 arranged in a second-dimensional array constituted of crossing lines and columns are provided on this device. Each large area 20 is provided with plural programmable logic areas 30 and a programmable memory area 40. Each logic area 30 is provided with plural small areas 50 constituted of programmable logics. Each large area 20 is provided with connected interconnection resources so that communication between the logics in the large area and the memory area 40 can be attained without using any huge inter-large area interconnection resources arranged on this device in the same way for relative local interconnection.



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